#4 2/4/04

Our Ref. No.: 004006.P001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Lee McBryde, et al.

Application No.: 09/882,471

Filed: June 14, 2001

For: **DATA MANAGEMENT ARCHITECTURE**

Examiner: Anthony T. Whittington

Art Unit: 2133

Mail Stop – FEE - AMENDMENTS
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

REQUEST FOR EXTENSION OF TIME

AND

RESPONSE TO OFFICE ACTION

Dear Commissioner:

This is in response to the outstanding Office Action mailed July 28, 2003. Reconsideration and withdrawal of the rejection of record is requested in view of the following remarks.

REMARKS

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by DeKoning et al.

As explained in Applicant's specification, in a RAID controller, placing the parity XOR engine on the host network side of the data cache maximizes data transfer bandwidth with minimum parity calculation overhead. This aspect of the invention, as defined in Claim 1 and shown, in Figure 3, allows for the use of pipelined register sets by which the XOR engine can calculate, check and correct any errors in real time during data transfers. This functionality is achieved by virtue of the pipelined architecture of the present invention as shown in Figure 3 as defined in Claim 1.